COPY

Remarks

By this Preliminary Amendment, claims 1, 6-8, 11-20 and 32-33 are amended and claims 21-31 and 34 are canceled without prejudice or disclaimer. Claims 35-40 are added. New figures are added, same as in the parent case, and the specification is amended accordingly. These amendments are intended as broadening amendments and are not meant to limit the scope of equivalents of the claims.

Claims 1-20, 32-33 and 35-40 are pending in this application.

Should the Examiner have any questions with regard to this submission, or determine that any further action is necessary to place this Application in better form for allowance, the Examiner is encouraged to telephone Applicants' representative at (202) 371-2600.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeffrey T. Helvey
Attorney for Applicants
Registration No. 44,757

Date: 7/24/03

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

Version With Markings To Show Changes/Amendments

In accordance with 37 CFR § 1.121(c), the following version of the claims and specification, as rewritten by the foregoing amendments, show the changes made relative to previous versions of the claims.

In the specification:

Please replace paragraph **[0001]** with the following:

--This application is a continuation of Application No. 10/359,201, filed on February 6, 2003, Titled: SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING, Inventors: van der GOES et al, which is a continuation of Application No. 10/158,773, filed on May 31, 2002, Titled: SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING, Inventors: van der Goes et al., which is a Continuation-in-Part of Application No. 10/153,709, Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER et al.; and is related to Application No. 10/158,774, Filed: May 31, 2002, Titled: ANALOG TO DIGITAL CONVERTER WITH INTERPOLATION OF REFERENCE LADDER, Inventors: MULDER et al; Application No. 10/158,595, Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER; and Application No. 10/158,193, Filed: May 31, 2002, Inventor: Jan MULDER; Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, Inventors: Jan MULDER et al., all of which are incorporated by reference herein.--

Please insert the following after paragraph [0024]:

--FIG. 10 shows the circuit of FIG. 2 with FET transistors used as switches.

FIG. 11 shows cascaded coarse and fine amplifier stages. --

Please amend paragraph [0028] as follows:

--In one embodiment, 30 coarse amplifiers, 30 coarse comparators, 19 fine amplifiers and 65 fine comparators are used.) The coarse amplifier A_C is connected to a capacitor C_1, which in turn is connected to either the output of a track-and-hold 101, or to V_{coarse} from the reference ladder 104. A two-phase clock, including phases ϕ_1 and ϕ_2, is used to control switches S_1, S_2 and S_3 of the coarse amplifier A_C. When the phase ϕ_1 is on, the switches S_2 and S_3 are closed, the switch S_1 is open. With the switch S_3 closed, the coarse ADC amplifier A_C is in a reset mode, and the capacitor C_1 is connected to the reference ladder tap V_{coarse}. Also on ϕ_1, the switch S_5 is closed, the switches S_4 and S_6 are open, and the fine capacitor C_2 is connected to an appropriate tap of the reference ladder V_{fine}. Note that all of the switches as S_1-S_6 are typically field effect transistor (FET) switches (see FIG. 10, where the switches are S_1-S_6 illustrated as FET devices). The switch S_3 may be referred to as a coarse ADC reset switch, and the switch S_6 may be referred to as a fine ADC reset switch. When the phase ϕ_1 of the two-phase clock is on, the switches S_3 and S_2 are closed, the amplifier A_C is in a reset mode, and the left side of the capacitor C_1 is connected to a tap of the reference ladder (i.e., V_{coarse}). The switch S_1 is open when ϕ_1 is on.--

Please amend paragraph [0043] as follows:

-- FIG. 4 further illustrates the operation of the amplifiers of the present invention in a situation where the fine ADC 105 has 4 cascaded stages (typically with a gain of 4x each), which are labeled GA, GB, GC and GD. (See FIG. 11, where two cascaded stages are shown for both fine and coarse amplifiers A_F and A_C, as one example.) In FIG. 4, the amplifier stage of the coarse ADC 102 is labeled GE, the coarse ADC comparator 107 is labeled CC, the fine ADC comparator 108 is labeled FC and the encoder is labeled ENC. The gray portions of FIG. 4 illustrate a progression of one sample's quantization down the amplifier cascade. First, the track-and-hold 101 is connected to the coarse ADC amplifier A_C, during phase ϕ_2. Meanwhile, the coarse comparator 107 (CC) is reset during ϕ_2. The fine ADC amplifier A_F stage GA is also reset. During the next phase ϕ_1, the first stage GA of the fine ADC 105 amplifies, while the second stage GB resets. The process continues, as the signal moves in

a pipelined manner down from GA to GB to GC to GD to the fine comparator 108 (FC), and ultimately to the encoder 106. The next quantization is directly behind the quantization just performed, moving from left to right in the figure, and offset by one clock cycle from the measurement illustrated in gray in FIG. 4.--

In the figures:

A corrected FIG. 4, and new FIGS. 10-11 are submitted.

In the claims:

Please cancel claims 21-31 and 34 without prejudice or disclaimer.

Please amend claims 1, 6-8, 11-20 and 32-33 as follows:

1. (Amended) An [N-bit] analog to digital converter (ADC) comprising:

[a reference ladder;]

a [track-and-hold] <u>first</u> amplifier tracking an input voltage with its output;

a coarse ADC amplifier connected to a coarse capacitor at its input and having a coarse ADC reset switch controlled by a first clock phase [of a two-phase clock];

a fine ADC amplifier connected to a fine capacitor at its input and having a fine ADC reset switch controlled by a second clock phase [of the two-phase clock], wherein [the track-and-hold amplifier is in a hold-mode during the second clock phase;

a switch matrix that selects] a [voltage subrange from the reference ladder] <u>set of reference voltages is selected</u> for use by the fine ADC amplifier based on an output of the coarse ADC amplifier,

wherein the coarse capacitor is charged to a coarse reference [ladder] voltage during the first clock phase and connected to the [T/H] <u>first amplifier's</u> output voltage during the second clock phase, and

wherein the fine capacitor is connected to a <u>fine reference</u> voltage [subrange] during the first clock phase and charged to the [track-and-hold] <u>first amplifier's</u> output

voltage during the second clock phase; and

an encoder that converts outputs of the coarse and fine ADC amplifiers to [an N-bit] a digital output.

6. (Amended) The analog to digital converter of claim 1, wherein the coarse capacitor is connected to the [track-and-hold amplifier] first amplifier's output on a delayed second phase.

7. (Amended) The analog to digital converter of claim 1, wherein the fine ADC capacitor is connected to the [track-and-hold amplifier] first amplifier's output on a delayed second clock phase and to the fine reference voltage [subrange] during a delayed first clock phase.

8. (Amended) The analog to digital converter of claim 1, further including a switch that connects an output of the [track-and-hold-] first amplifier to the coarse capacitor on the second clock phase.

11. (Amended) An [N-bit] analog to digital converter comprising:

[a reference ladder;]

a track-and-hold amplifier tracking an input voltage;

[a two-phase clock having phases ϕ_1 and ϕ_2;]

a first plurality of [coarse ADC] amplifiers each connected to a corresponding [coarse] capacitor at its input, wherein the [coarse ADC] amplifiers of the first plurality are reset on a clock phase ϕ_1 and their corresponding [coarse] capacitors are connected to an output of the track-and-hold on a clock phase ϕ_2[, and wherein the track-and-hold amplifier is in a hold-mode on ϕ_2];

a second plurality of [fine ADC] amplifiers each connected to a corresponding [fine] capacitor at its input, wherein the [fine ADC] amplifiers of the second plurality are reset on the clock phase ϕ_2 and their corresponding [fine] capacitors are charged to the track-and-hold amplifier output voltage on the clock phase ϕ_2[;

a switch matrix that selects] and wherein a [voltage subrange from the reference

ladder,] set of reference voltages is selected based on outputs of the [coarse ADC] first plurality of amplifiers, for input to the [fine ADC] second plurality of amplifiers on the clock phase ϕ_1; and

an encoder that converts outputs of the [coarse and fine ADC] first and second pluralities of amplifiers to [an N-bit] a digital output.

21. (Amended) The analog to digital converter of claim 11, further including [a] FET [switch] switches that [resets] reset the [coarse ADC amplifier] first plurality of amplifiers on the clock phase ϕ_1.

22. (Amended) The analog to digital converter of claim 11, wherein the clock phases ϕ_1 and ϕ_2 [phases] are non-overlapping.

23. (Amended) The analog to digital converter of claim 11, wherein each of the [fine ADC] second plurality of amplifiers [include] includes a plurality of cascaded amplifier stages.

24. (Amended) The analog to digital converter of claim 11, wherein each of the [coarse ADC] first plurality of amplifiers [include] includes a plurality of cascaded amplifier stages.

25. (Amended) The analog to digital converter of claim 11, wherein the [coarse] capacitors of the first plurality of amplifiers are connected to the track-and-hold amplifier output on a delayed clock phase ϕ_2.

26. (Amended) The analog to digital converter of claim 11, wherein the [fine] capacitors of the second plurality of amplifiers are connected to the track-and-hold amplifier output on a delayed clock phase ϕ_2, and to the [voltage subrange] set of reference voltages on a delayed clock phase ϕ_1.

27. (Amended) The analog to digital converter of claim 11, further including switches that

connect an output of the track-and-hold to the [coarse] capacitors of the first plurality of amplifiers on the clock phase ϕ_2.

28. (Amended) The analog to digital converter of claim 11, further including a first plurality of [coarse] comparators that latch the outputs of the [coarse ADC] first plurality of amplifiers and output them to the encoder.

29. (Amended) The analog to digital converter of claim [11] 19, further including a second plurality of [fine] comparators that latch the outputs of the [fine ADC] second plurality of amplifiers and output them to the encoder.

32. (Amended) An [N-bit] analog to digital converter comprising:

[a two-phase clock having phases ϕ_1 and ϕ_2;]

[a reference ladder;]

a track-and-hold amplifier tracking an input voltage;

a [coarse ADC] first amplifier that resets on a clock phase ϕ_1 and amplifies a difference of an output of the track-and-hold amplifier and a [coarse tap of the] first voltage reference [ladder] on a clock phase ϕ_2 [, wherein the track-and-hold amplifier is in a hold-mode];

a [fine ADC] second amplifier that resets on the clock phase ϕ_2 and amplifies a difference of the output of the track-and-hold amplifier and a [fine tap of the] second reference [ladder] voltage on the clock phase ϕ_1[;

a switch matrix that selects], wherein a [voltage subrange from the] first set of reference [ladder] voltages is selected for use by the [fine ADC] second amplifier based on an output of the [coarse ADC] first amplifier; and

an encoder that converts outputs of the [coarse and fine ADC] first and second amplifiers to [an N-bit] a digital output.

33. (Amended) A method of converting an analog voltage to a digital voltage comprising the steps of:

resetting a [coarse ADC] first amplifier on [the] a first clock phase;

COPY

charging a [coarse] first capacitor to a first reference voltage during [a] the first clock phase [of a two phase clock];

connecting the [coarse] first capacitor to an input voltage during a second clock phase [of the two phase clock;], wherein [the T/H] a track-and-hold amplifier is in a hold-mode during the [2nd] second clock phase;

selecting [the] a second reference voltage based on an output of the [coarse ADC] first amplifier;

connecting a [fine] second capacitor to [a] the second reference voltage during the first clock phase;

charging the [fine] second capacitor to the input voltage during the second clock phase;

amplifying a voltage on the [coarse] first capacitor on the second clock phase;

resetting a [fine ADC] second amplifier on the second clock phase;

amplifying a voltage of the [fine] second capacitor on the first clock phase; and

converting outputs of the [coarse] first and [fine ADC] second amplifiers to [an N-bit] a digital output.

147614_1